- Page 10, lines 17-19
- Page 10, lines 23-25
- Page 11, lines 1-7
- Page 11, lines 16-19

IN THE ABSTRACT:

Please amend the abstract as indicated by the clean copy of the amended abstract in Appendix D, and the marked-up copy of the amended abstract in Appendix E, attached hereto.

IN THE DRAWINGS:

Please amend Fig. 2 to include reference $C_d(2)$ for the capacitor next to $g_m V(2)$, as marked in red on the copy of Fig. 2 attached hereto for approval by the Examiner.

Please amend Fig. 8 by changing reference "Ld/2" to –L– for the four indicators at the top of the circuit, as marked in red on the copy of Fig. 8, attached hereto by the Examiner.

Please add new Fig. 9, attached hereto for approval by the Examiner.

In addition, a complete set of formal drawings including the above-mentioned changes is attached.

REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Objections to Specification

The objections to the specification set forth on page 2 of the Official Action have been addressed by:

(i) Adding Fig. 9 to correspond to the description of Fig. 9 in lines 23-25 on page 9, and beginning in line 23 on page 10, as suggested in item (1) of the objections, (new Fig. 9 being identical to the corresponding Fig. 9 of the priority application); and

(ii) Correcting the typographical error in line 17 on page 11.

2. Objection to the Drawings

This objection has been addressed by adding Fig. 9, as indicated above, and by amending the page 2, lines 8 and 23 of the specification to refer to Cgd rather than Cds. In addition, the un-numbered capacitor in Fig. 2 has been labeled as Cd(2), consistent with the labeling of capacitor Cd(1).

3. Rejection of Claims 2-3 Under 35 USC §112, 2nd Paragraph

This rejection has been addressed by re-writing claims 2 and 3 as new claims 5 and 6 to clarify that the distance between drain terminals is L_d, as explained in lines 23-25 on page 10 of the original specification, and that the capacitances are located, relative to a respective drain terminal, some fraction xL_d or $(1-x)L_d$ of the distance L_d between the drain terminals. The Examiner will note that the location of the capacitance is given by xL_d or $(1-x)L_d$, and not by x itself. The variable x is not a location, but rather simply gives the fraction of the distance L_d at which the capacitances are located.

Because the distance of the capacitances from corresponding drain terminals are defined as xL_d or $(1-x)L_d$, x inherently must be between 0 and 1 since the distance from the drain line to the capacitance is 0 at x=0, and Ld at x=1. If x were greater than 1, the first capacitance would not be ***between*** the drain lines. As a result, claim 5 also includes a recitation that $0<x<1$.

In addition, the "0.5" language of claim 3 has been modified to point out that the preferred lengths of the drain lines is $-0.5L_d-$, which is half the distance between the FETs, as shown in Fig. 9, and explained in lines 16-19 on page 11 of the original specification ("*Although*

the location of the additional capacitance can be anywhere in the drain line, . . ., it is most effective in optimizing the gain-bandwidth product of traveling-wave amplifier having Π-type drain transmission line structure when the x value is 0.5."). Fig. 8 has also been amended for consistency, as has the paragraphs bridging pages 10 and 11 of the original specification.

4. Rejection of Claims 1 and 2 Under 35 USC §102(b) in view of U.S. Patent No. 5,046,155 (Beyer), and Rejection of Claim 3 Under 35 USC §103(a) in view of Beyer

The rejections of claims 1 and 2 under 35 USC §102(b) and of claim 3 under 35 USC §103(a) are respectfully traversed on the grounds that the Beyer patent neither discloses nor suggests a traveling wave amplifier in which an additional capacitance is added between **drain** lines connected to the **drain** terminals of respective FETs to match **phase velocities** between input (gate) and output (drain) lines and thereby improve **gain characteristics**, as claimed. Instead, Beyer adds capacitances Cs1 and Cp1, Cs2 and Cp2, *etc.*, to the **gate** inputs of FETs 1,2,3, *etc.*, and T-sections to both the input and output transmission lines to shift the minimization bandwidth to lower frequencies and thereby **improve the directivity** (reduce S_{41} relative to S_{31} or *vice versa*).

It is respectfully noted that support for the recitation of input/output phase velocity matching is found, for example, in lines 7-18 on page 3 of the original specification, which points out that

> *. . .the gain-bandwidth product of a traveling-wave amplifier can be maximized when the velocity of a traveling-wave signal propagating in the input transmission line (i.e. the gate line in case of traveling-wave amplifier using FETs) and the velocity of output traveling-wave signal propagating in the output transmission line (i.e. the drain line in case of traveling-wave amplifier using FETs) are matched.*

In contrast, Beyer seeks an essentially opposite result, namely increased directivity through "binomial scaling," which is why Beyer places "additional" capacitances on the output transmission lines.

As a result, the amplifiers of Beyer and the claimed invention are, at least, distinguishable for the following reasons:

(i) the improvements taught by Beyer have a different purpose than those of the claimed invention, *i.e.*, improved directivity versus improve gain characteristics (bandwidth and ripple of S_{21} in the present application and S_{41} of Beyer), and

(ii) the improvements of Beyer are implemented in a different manner than those of the claimed invention, *i.e.*, by means of "binomial scaling" using capacitances Cs1 and Cp1, Cs2 and Cp2, *etc.* connected to the FET **gate** inputs, and the addition of passive T-sections to the amplifier inputs and outputs, rather than by connecting additional capacitances between or to the respective **drain** lines, as claimed.

In contrast to the amplifier of Beyer, the present invention provides a traveling-wave amplifier having a Π-type output transmission line structure, in which the additional capacitance used for velocity matching of the input/output transmission lines is connected in the middle of the output line. Since the additional element is isolated from the output of the transistor by the output transmission line, the Π-type output transmission line structure of the invention can achieve velocity matching of output/input transmission lines without the stability problem normally associated with an additional capacitance and the feedback capacitances of the transistor. The traveling-wave amplifier of the claimed invention therefore has an improved bandwidth, gain flatness, and stability compared to traveling-wave amplifiers having the conventional output line structures, as well as compared to the amplifier disclosed in the Beyer patent.

In addition to providing improved gain characteristics such as gain ripple and bandwidth, rather than directivity, the positively recited structural differences between the traveling wave amplifier of Beyer and that of the claimed invention have the consequence that Beyer's amplifier is larger than that of the claimed invention, because Beyer's addition of the passive T-sections causes the lengths of the input and output transmission lines of Beyer to be increased to 2Lg and

2Ld respectively, as opposed to Ld in the present application (and the illustrated "prior art" amplifier).

In addition, the Examiner will note that the capacitance values in the passive T-sections shown in Fig. 8 of Beyer are **identical** to those of the respective FETs, *i.e.*, Cds/2 for output and Cgs/2 for input, whereas the value of the claimed additional capacitance is clearly **different** from the capacitance values of the claimed FETs. Although specific capacitance values have not been claimed, the difference in capacitance values is evidence of the fundamentally different natures of the claimed amplifier and that of Beyer.

It is respectfully submitted that the location of the T-sections in Beyer is highly significant, and cannot be discounted either for purposes of anticipation or obviousness. Instead, since T-sections in general are well-known, the specific structure of the T-sections of Beyer must have been critical to achieving the objective of improved directivity. Consequently, it cannot be said that the ordinary artisan would simply have re-arranged those sections to obtain the claimed invention without some explicit, or at least strongly implied, teaching to do so. As explained in **MPEP 2143.02**:

> *If the proposed modification or combination of the prior art would* ***change the principle of operation of the prior art invention being modified****, then the teachings of the references are not sufficient to render the claims prima facie obvious* (citing In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)...*The court reversed the rejection holding the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference]* ***as well as a change in the basic principle under which the [primary reference] construction was designed to operate****" 123 USPQ at 352.*

In conclusion, because the Beyer patent fails to disclose or suggest the presently claimed first and second additional capacitances connected to the drain lines for the purpose of improving gain characteristics, including reducing gain ripple and increasing bandwidth, it is respectfully submitted that the Beyer patent, whether considered individually or in combination with any of

the other references of record, neither anticipates nor renders obvious the claimed invention, and withdrawal of the rejections under 35 USC §§102(b) and 103(a) is respectfully requested..

Having thus overcome each of the rejections made in the Official Action, expedited passage of the application to issue is requested.

Respectfully submitted,
BACON & THOMAS, PLLC

Date: March 26, 2002

By: BENJAMIN E. URCIA
Registration No. 33,805

BACON & THOMAS, PLLC
625 Slaters Lane, 4th Floor
Alexandria, Virginia 22314
Telephone: (703) 683-0500

NWB:S:\Prodocerben\Pending Q...ZS\SONG756772w01.wpd

APPENDIX A
(New Claims)

4. (New) A traveling-wave amplifier, comprising:

an input transmission line including first, second, third, and fourth drain lines;

an output transmission line including first, and second gate lines;

a first FET having a drain terminal connected between said first and second drain lines and a gate terminal connected to said first gate line;

a second FET having a drain terminal connected between said third and fourth drain lines and a gate terminal connected between said first and second gate lines;

a first additional capacitance connected between said second and third drain lines; and

a second additional capacitance connected to the fourth drain line,

wherein said first and second capacitances are arranged to match phase velocities of signals in said input transmission line with phase velocities of signals in said output transmission line and thereby improve gain characteristics by reducing gain ripple and increasing bandwidth.

5. (New) A traveling-wave amplifier as claimed in claim 4, wherein:

L_d is a distance between said drain terminals of the first and second FETs,

$(1-x)L_d$, $0<x<1$, is a length of said first and third drain lines,

xL_d, $0<x<1$, is a length of said second and fourth drain lines,

said first additional capacitance is located a distance xL_d from the drain terminal of said first FET and a distance $(1-x)L_d$ from the drain terminal of said second FET, and

said second additional capacitance is located a distance xL_d from the drain terminal of said second FET.

6. (Amended) A traveling-wave amplifier as claimed in claim 5, wherein $x = 0.5$.

APPENDIX B
(Clean Copy Of Amended Paragraphs)

Page 2, lines 4-10:

In this case, however, the gain is increased, but the bandwidth is decreased. Thus, the expected gain-bandwidth product improvement cannot be achieved. The bandwidth of the ordinary amplifiers in which transistors are connected in parallel is decreased because capacitances(C_g, C_d, and C_{gd}) shown in Fig. 2, the small signal equivalent circuit of the FET circuit of Fig. 1 are increased in proportion to the number of transistors that are simply connected in parallel.

Page 2, lines 19-21:

If transistors are connected in the way shown in Fig. 1, the total gain of the amplifier is increased in proportion to the number of transistors, as is evident from the small signal equivalent circuit illustrated in Fig. 2.

Page 2, line 22 to page 3, line 6:

Unlike the ordinary amplifiers where the unit transistors are simply connected in parallel, the capacitances(C_g, C_d, and C_{gd}) are separated by the transmission lines in the traveling-wave amplifier. Since these capacitances are separated by the transmission lines, the effective capacitances seen from the input and output of the unit transistors are not increased in proportion to the number of unit transistors. Therefore, the bandwidth of the individual unit transistors as well as the traveling-wave amplifier is not decreased. Thus, improved gain-bandwidth product of the traveling-wave amplifier can be obtained.

Page 3, lines 14-18:

In a traveling-wave amplifier without velocity matching, as illustrated in FIGS. 1 and 2, the input/output transmission lines (indicated as L_g and L_d) are simply connected to the input/output of unit transistors. In this structure, input/output impedances are determined by the following equations.

Page 4, lines 11-14:

An example of small signal equivalent circuit parameter values for the small signal equivalent circuit of FIG. 2 using a typical FET (gallium arsenide FET) is shown in Table 1.

Page 10, lines 14-16:

In FIG. 8, the drain terminal of FET(1) is connected between drain line $L_d(1)$ and $L_d(2)$, and the additional capacitance $C_3(1)$ is connected between drain line $L_d(2)$ and $L_d(3)$.

Page 10, lines 17-19:

Also, the drain terminal of FET(2) is connected between drain line $L_d(3)$ and $L_d(4)$, and the additional capacitance $C_3(2)$ is connected to the drain line $L_d(4)$.

Page 10, lines 23-25:

As shown in FIG. 9, the total length of drain line between the drain terminals of the said FET(1) and FET(2) is represented as L_d, and the length of drain lines $L_d(1)$ and $L_d(3)$ is $(1-x)L_d$ and that of $L_d(2)$ and $L_d(4)$ is (x)Ld, respectively, where x is the number larger than 0 and smaller than 1 ($0<x<1$).

Page 11, lines 1-7:

While the additional capacitances or inductances for velocity matching of the conventional drain line structures are connected directly to the drain of unit transistors, the additional capacitance (C_3) in the Π-type drain line structure is not directly connected to the output(drain) of unit transistors. Instead, it is isolated from the output(drain) of the unit transistor by drain transmission lines (e.g. $L_d(1)$, $L_d(2)$, $L_d(3)$, and $L_d(4)$) as shown in FIG. 8 and 9.

Page 11, lines 16-19

Although the location of the additional capacitance can be anywhere in the drain line (i.e., $0<x<1$ in Fig. 9), it is most effective in optimizing the gain-bandwidth product of traveling-wave amplifier having Π-type drain transmission line structure when the x value is 0.5.

APPENDIX C
(Marked-Up Copy Of Amended Paragraphs)

Page 2, lines 4-10:

In this case, however, the gain is increased, but the bandwidth is decreased. Thus, the expected gain-bandwidth product improvement cannot be achieved. The bandwidth of the ordinary amplifiers in which transistors are connected in parallel is decreased because capacitances(C_g, C_d, and [C_{ds}] C_{gd}) shown in Fig. 2, the small signal equivalent circuit of the FET circuit of Fig. 1 are increased in proportion to the number of transistors that are simply connected in parallel.

Page 2, lines 19-21:

If transistors are connected in the way shown in Fig. 1, the total gain of the amplifier is increased in proportion to the number of transistors, as is evident from the small signal equivalent circuit illustrated in Fig. 2.

Page 2, line 22 to page 3, line 6:

Unlike the ordinary amplifiers where the unit transistors are simply connected in parallel, the capacitances(C_g, C_d, and [C_{ds}] C_{gd}) are separated by the transmission lines in the traveling-wave amplifier. Since these capacitances are separated by the transmission lines, the effective capacitances seen from the input and output of the unit transistors are not increased in proportion to the number of unit transistors. Therefore, the bandwidth of the individual unit transistors as well as the traveling-wave amplifier is not decreased. Thus, improved gain-bandwidth product of the traveling-wave amplifier can be obtained.

Page 3, lines 14-18:

In [FIG. 1,] a traveling-wave amplifier without velocity matching [is], as illustrated in FIGS. 1 and 2, the [The] input/output transmission lines ([These are] indicated as L_g and L_d) are simply connected to the input/output of unit transistors. In this structure, input/output impedances are determined by the following equations.

Page 4, lines 11-14:

[FIG. 2 is a small signal equivalent circuit of FET that is used for traveling-wave amplifiers.] An example of small signal equivalent circuit parameter values [of] for the small signal equivalent circuit of FIG. 2 using a typical FET (gallium arsenide FET) is shown in Table 1.

Page 10, lines 14-16:

In FIG. 8, the drain terminal of FET(1) is connected between drain line [L_d/2(1)] L_d(1) and [L_d/2(2)] L_d(2), and the additional capacitance C_3(1) is connected between drain line [L_d/2(2)] L_d(2) and [L_d/2(3)] L_d(3).

Page 10, lines 17-19:

Also, the drain terminal of FET(2) is connected between drain line [L_d/2(3)] L_d(3) and [L_d/2(4)] L_d(4), and the additional capacitance C_3(2) is connected to the drain line [L_d/2(4)] L_d(4).

Page 10, lines 23-25:

[The] As shown in FIG. 9, the total length of drain line between the drain terminals of the said FET(1) and FET(2) is represented as L_d, and the length of drain lines [L_d/2(1)] L_d(1) and [L_d/2(3)] L_d(3) is (1-x)L_d and that of [L_d/2(2)] L_d(2) and [L_d/2(4)] L_d(4) is (x)Ld, respectively, where x is the number larger than 0 and smaller than 1 ($0<x<1$).

Page 11, lines 1-7:

While the additional capacitances or inductances for velocity matching of the conventional drain line structures are connected directly to the drain of unit transistors, the additional capacitance (C_3) in the Π-type drain line structure is not directly connected to the output(drain) of unit transistors. Instead, it is isolated from the output(drain) of the unit transistor by drain transmission lines (e.g. [L_d/2(1), L_d/2(2), L_d/2(3), and L_d/2(4)] L_d(1), L_d(2), L_d(3), and L_d(4)) as shown in FIG. 8 and 9.

Page 11, lines 16-19

[The] Although the location of the additional capacitance can be anywhere in the drain line (i.e., [0<x<0] 0≤x≤1 in Fig. 9), [. hoever] it is most effective in optimizing the gain-bandwidth product of traveling-wave amplifier having Π-type drain transmission line structure when the x value is 0.5.

APPENDIX D

(Clean Copy of Amended Abstract)

The present invention relates to a traveling-wave amplifier having a Π-type output transmission line structure. In traveling-wave amplifiers having conventional output line structures including T-line and m-derived-line structures, additional capacitance and inductance are attached to the output of the transistors for velocity matching in input/output transmission lines in order to improve gain-bandwidth product. However, it is difficult to achieve velocity matching of output/input transmission lines without stability problems due to the influence of the additional capacitance and inductance through the feedback capacitance of the transistor used. The present invention provides a traveling-wave amplifier having a Π-type output transmission line structure, where the additional capacitance used for velocity matching of the input/output transmission lines is connected in the middle of the output line. Since the additional element is isolated from the output of the transistor by the output transmission line, the Π-type output transmission line structure can achieve velocity matching of output/input transmission lines without stability problems associated with the additional capacitance and the feedback capacitance of the transistor. The traveling-wave amplifier having a Π-type output transmission line structure has an improved bandwidth, gain flatness, and stability compared to traveling-wave amplifiers having the conventional output line structures.

APPENDIX E
(Marked-Up Copy Of Amended Abstract)

The present invention relates to [the] a traveling-wave amplifier having a Π-type output transmission line structure.[

]In traveling-wave amplifiers having conventional output line structures including T-line and m-derived-line structures, additional capacitance and inductance are attached to the output of the transistors for velocity matching in input/output transmission lines in order to improve gain-bandwidth product. However, it is difficult to achieve velocity matching of output/input transmission lines without stability [problem] problems due to the influence of the additional capacitance and inductance through the feedback capacitance of the transistor used.[

]The present invention provides [the] a traveling-wave amplifier having a Π-type output transmission line structure, where the additional capacitance used for velocity matching of the input/output transmission lines is connected in the middle of the output line. Since the additional element is isolated from the output of the transistor by the output transmission line, the Π-type output transmission line structure can achieve velocity matching of output/input transmission lines without stability [problem] problems associated with the additional capacitance and the feedback capacitance of the transistor. The traveling-wave amplifier having a Π-type output transmission line structure has an improved bandwidth, gain flatness, and stability compared to traveling-wave amplifiers having the conventional output line structures.

APPROVED
FOR ENTRY
5/17/02
DT

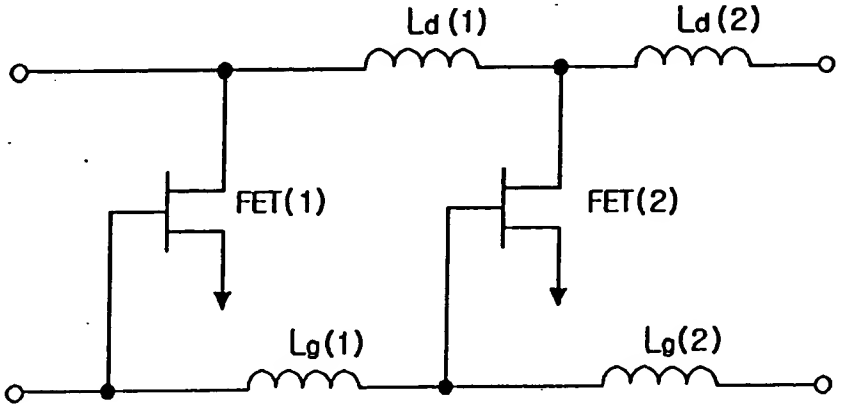

FIG. 1

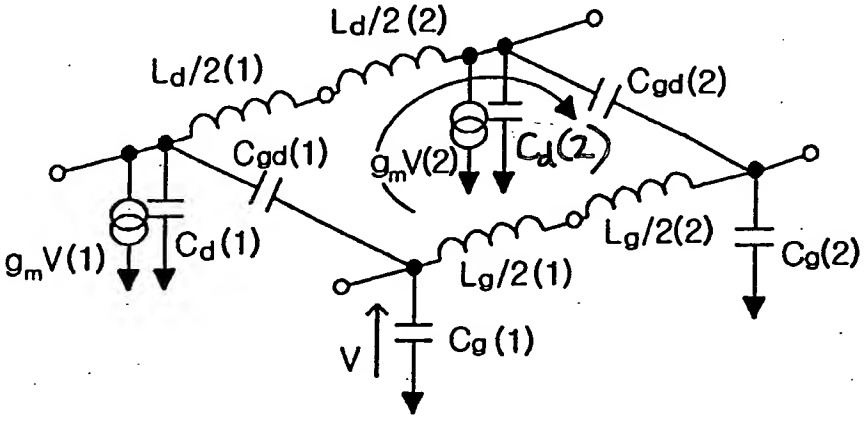

FIG. 2

Approved for entry 5/17/02 DT

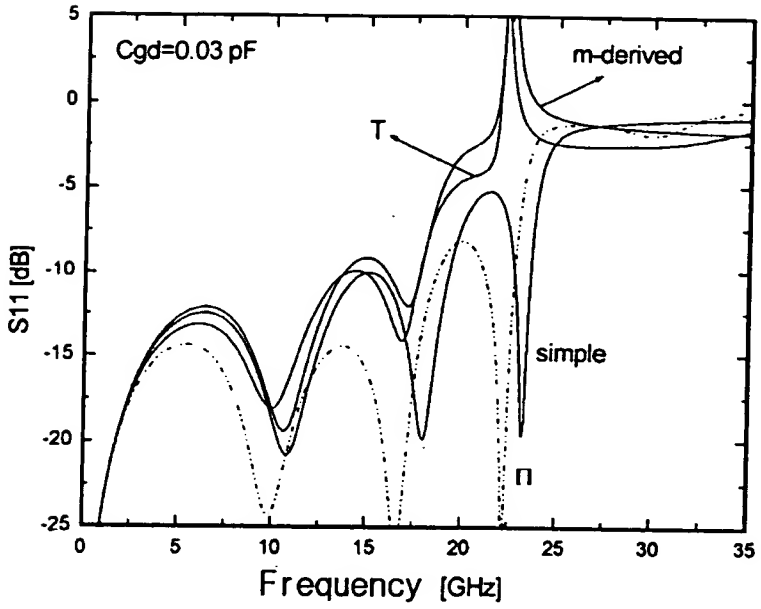

FIG. 7

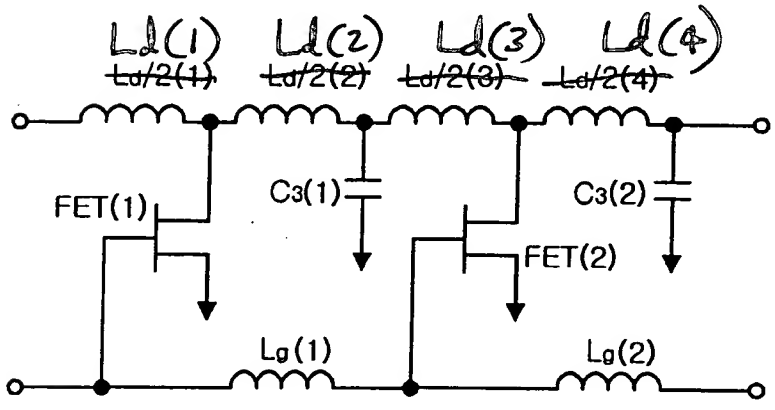

FIG. 8

Approved for entry
5/17/02
DT

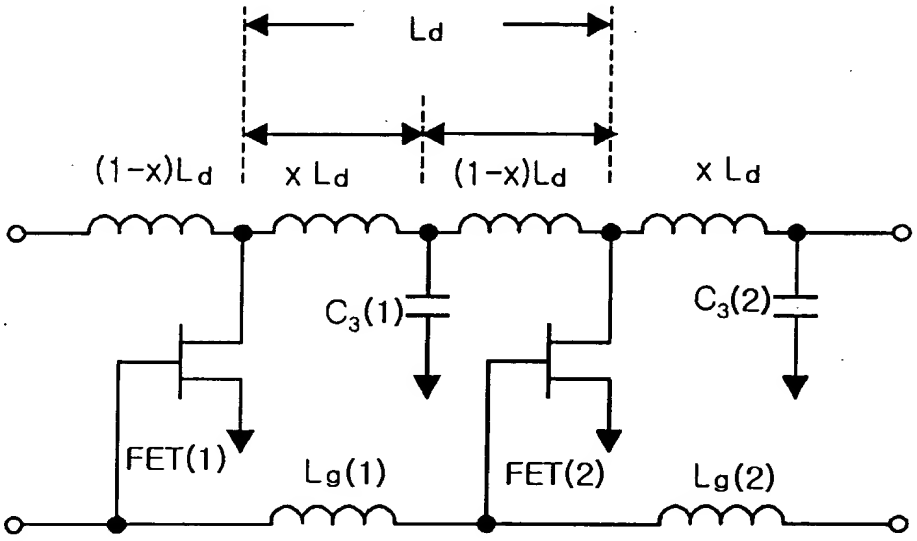

Fig. 9